American Journal of Technology Advancement 2997-9382, Vol 3, No.2 (Feb, 2026).

Article

A Critical Review of Next-Generation Semiconductor Devices Progress in Fabrication Techniques, Reliability, and Application Domains

Sarmad Hamad Ibrahim Alfarag
Electrical Engineering Department, Wasit University, Wasit, Iraq
Email: Sarmad.hamad@uowasit.edu.iq

Abstract: This review critically analyzes recent developments in state-of-the-art semiconductor devices with particular focus on how the architecture, fabrication technologies and reliability constraints depend on each other. IEEE Xplore, ScienceDirect, SpringerLink, Nature Portfolio journals, and ACS Publications were used as sources of structured literature review on the topic of the study, concentrating on the peer-reviewed articles that present the performance of the devices, fabrication integration, and a reliability behavior. The review presents an overview of the advances in the main types of devices such as gate-all-around field-effect transistors (GAAFETs), complementary FETs (CFETs), two-dimensional (2D) material transistors, wide-bandgap GaN and SiC power devices, and memristive/neuromorphic systems. The results reveal that GAAFET implementations provide obvious advantages in control of leakage as well as electrostatic, however such advantages are less and less with respect to fabrication delicatenesses, self-heating, and stacked channel variation. FETs Two-dimensional FETs have a high theoretical scalability but are limited by contact resistance, reproducibility at the wafer scale and stability in operation. Conversely, technological maturity and dominance of power and automotive in applications are found in the case of GaN and SiC devices, even though reliability issues of trapping and oxide degradation of gates remain a significant problem. The application of memristive devices in edges artificial intelligence and neuromorphic computing is promising, but its usage is hindered by the lack of endurance variability and variability in stochastic switching to scale to large scale. The review finds that reliability has become the most critical bottleneck below the 3-nm scale, with monolithic three-dimensional integration, new materials, and AI-assisted predictive reliability modeling being the way forward to continue with semiconductor innovation in the future.

Keywords: Zero-dose children, urban–rural gap, vaccination coverage, regional disparities, declining trend, access inequality, immunization gaps.

This is an open-access article under the CC-BY 4.0 license

1. Introduction

The further extension of the Moore law has become not a dimensional scaling issue but a co-optimization problem of significantly limited nature of device architecture, fabrication accuracy and reliability physics. Traditional planar CMOS and, later, FinFET designs were allowing decades of scaling in performance, but with critical dimensions reaching the sub-3-nm regime, there was a growing increase in the limitations of alternate performance by electrostatic integrity, power density, and variability [1]. Such limitations have prompted the development of gate-all-around field-effect transistors (GAAFETs), and the study of two-dimensional (2D)-channel semiconductor channels and

wide-bandgap (GaN and SiC) technology to be used on an application basis, in place of universal CMOS.

GAAFET architecture gives better control of the electrostatics of the channel since the entire gate is encased in total channel cover, thus allows minimization of leakage and improved short-channel characteristics [2]. Nevertheless, at the cost of a much-greater sensitivity to fabrication, such benefits are realized at the cost of stacked nanosheet implementations where the channel release, spacer formation and interface quality have to be realized with atomic-scale accuracy. Simultaneously, 2D-FETs in theory, provide maximum thickness scaling and insensitivity to short-channel effects, but experimental investigations show that there are still significant issues in terms of contact resistance, wafer-scale uniformity, and stability of operation, which make them difficult to produce in the near future. In contrast, devices based on GaN and SiC have become more technologically mature in the fields of power and automotive electronics, where integration density is less important than in others, and defect- and trapping-induced degradation is an urgent reliability issue [3]. The chart below shows the global GaN and SiC power semiconductor market growing rapidly at an 18.3% CAGR, rising from about $1.42 billion in 2024 to $3.29 billion by 2029.

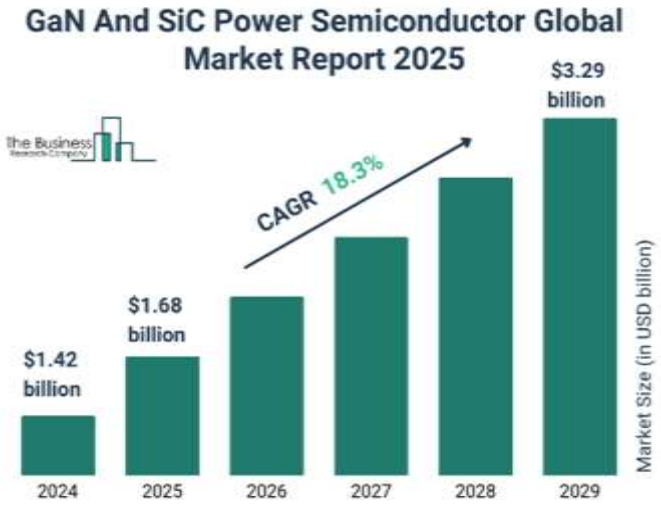


Figure 1. Global GaN and SiC power semiconductor market growth (Research Company, 2025)

The achievement of these advanced architectures cannot be made possible without the escalation of reliance on extreme ultraviolet (EUV) lithography, atomic layer deposition (ALD) and high selectivity patterning methods. Although they allow a previously unseen level of dimensional control, they create small process windows and stochastic variability, which increases the sensitivity of defects and becomes sensitive to degradation processes. As a result, such phenomena as reliability temperature instability (BTI) [4], self-injection (HCI), time-dependent dielectric breakdown (TDDB) [5], and self-heating have become the essential limitations, and tend to counterbalance the increasing nominal performance gains in aggressively scaled devices [6].

In this context, the current review deals with two key goals. To start with, it critically assesses the conversion of current developments in device architecture and fabrication technologies into real performance, scalability, and energy efficiency enhancement (Aim 1; RQ1). Second, it studies the essence of reliability mechanisms that portrays the application readiness of emerging semiconductor devices in the logic, power, and intelligent computing fields (Aim 2; RQ2). This work has related reliability as a resounding element of deciding the next generation path of next-generation semiconductor technologies by engineering evidence across architectures, processes, and degradation physics.

Objectives of the Study

1. Objective 1: Assess the current developments in semiconductor devices and their architectures and manufacturing processes and the effect of these developments on their performance and

scalability.

2. Objective 2: Examine significant issues of reliability and evaluate their contribution to the applicability of the new device technologies.

Research Questions

3. RQ1: In what ways have developing technologies of architecture and fabrication enhanced the performance, scalability, and efficiency in next-generation semiconductor devices?
4. RQ2: Which mechanisms of reliability impact the emerging semiconductor devices, and how these issues affect preparedness in the critical application fields?

2. Materials and Method

Literature Review (Thematic)

Section 5.1 of the plan focuses on the evolution of the device architecture of the system.

The architectural development of FinFETs into GAAFETs and finally CFETs is a change of lateral to vertical scaling of the electrostatic integrity as the latter limits the architectures at lower nodes. FinFETs had a fin-length CMOS-expansion of the performance, though the variability of the fin width and parasitic resistance to advantages rises below reasonably 7 nm [7], [8]. GAAFETs, and especially implementation in nanosheet form, overcome these shortcomings by allowing full enclosing the gate, and adjusting the channel width, which leads to enhanced short-channel control, reduced leakage currents [9]. However, stacked nanosheet designs create a great deal of sensitivity to variability due to fabrication and self-heating, limiting the scale of voltages and frequencies [10]. The figure below illustrates how GAAFETs fully surround the channel with the gate—unlike FinFETs—enabling adjustable nanosheet widths that deliver stronger short-channel control and significantly reduced leakage currents.

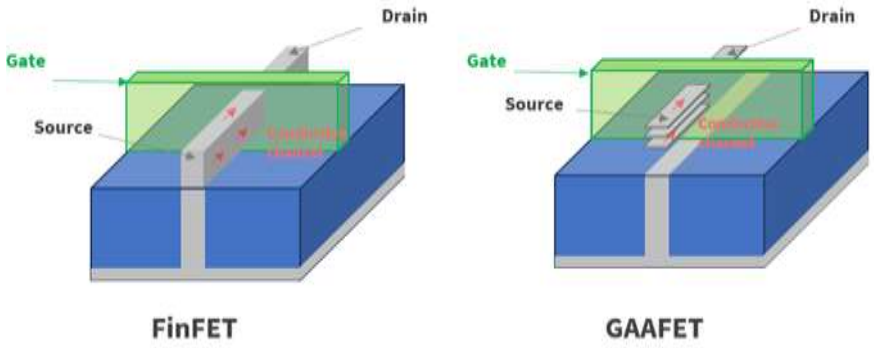


Figure 2. FinFet vs Gaafet [11]

As a way of scaling density scaling beyond the constraints of planar layout optimization, complementary FETs (CFETs) are vertically stacked n-type and p-type devices to provide a significant reduction in footprint [12]. In spite of their theoretical density edge, CFETs are still limited by compatibility with process and thermal conductivity, as well as by stacked levels of cumulative reliability challenges [13].

Similar to CMOS development, 2D (two-dimensional) material FETs have been considered as ultimate-body-thickness channels that can are able to suppress the short-channel effect [14]. Although recent demonstrations have demonstrated demonstration of promising subthreshold slopes and scalability to the electrostatic scale, contact resistance, interface instability, and inability to achieve uniformity at the wafer scale are limiting issues to large-scale implementation [15].

Conversely, the power devices that are based on GaN and SiC focus on the high breakdown voltage and efficiency rather than a density scaling [16]. Their swift commercial implementation in energy and automotive electronics shows that there has been an effective allusion between the characteristics of materials and the specifications of the applications, although issues regarding the level

of defects and durability remain undefeated.

Lastly, neuromorphic and memristive devices are a paradigm shift of Boolean scaling to in-memory design and brain-inspired design. Even though they show great capabilities in AI workloads, the variability in devices and endurance are significant obstacles to system-level implementations [17].

Fabrication Techniques

The architectures of advanced devices cannot be discussed outside of the context of fabrication development, especially, the growing use of extreme ultraviolet (EUV) lithography [18]. EUV has made it possible to single-pattern at critical dimensions as small as 20 nm, but with reduced overlay errors and complexity, stochastic defects, resist variability, and increased cost complexity have made it difficult to scale in the long run [19]. These constraints are even accentuated whilst device architectures require stricter tolerances and pattern fidelity.

Angstrom-level control and conformality Angstrom level thickness and conformability Angstrom-level thickness and conformality Due to its ability to achieve angstrom level control and conformability, atomic layer deposition (ALD) has become a foundational process in next-generation devices. In GAAFETs and 3D structures, gate stacks, spacers, and interfacial layers can critically rely on ALD, but there are limited and narrow process windows and precursor constraints, which negatively impact throughput and defectivity [20].

Equally, nanosheet release and CFET integration are based on selective etching and deposition methods. Although high selectivity results in high material removal accuracy, it increases sensitivity to changes in local composition, which create variability and loss of yield [21].

In addition to front-end processes 3D heterogeneous integration, such as chiplets, new advanced packaging and options of emerging mono-3D systems, are now considerations of strategic alternative to classical scaling. These will enhance the performance at the system level but will result in the emergence of new thermal and reliability interactions between stacked layers [22].

Performance Aspects

The next generation devices are beginning to gain improvements on performance on the basis of electrostatic control instead of pure dimensional scaling. GAAFETs have lower leakage and better subthreshold characteristics than FinFETs and switching speed benefits are usually canceled by the parasitic resistance and capacitance in complex 3D designs [23].

In 2D-FETs, intrinsic carrier mobility is enticing, but extrinsic ones most significantly influence the overall device behavior, especially, contact resistance. In the case of GaN and SiC devices, the benefits in performance take the form of energy efficiency and hasty operation, allowing the gain at system-level, as opposed to density of the transistor [24].

Cross-cutting performance limiter has come out in form of thermal management. With a higher power density in vertically integrated devices, heat dissipation limits are becoming a bottleneck to performance even with the electrical characteristics remaining desirable [25].

3. Result

Reliability Mechanisms

Reliability has now become a second-rate consideration when it relates to qualification and a first-rate scaling bottleneck. A bias temperature instability (BTI) currently is the leading cause of degradation in advanced CMOS and GAAFETS, even in the presence of high-k dielectrics and interface defect density. Hot-carrier injection (HCI) remains a high-field phenomenon, whereas time-dependent dielectric breakdown (TDDB) puts a growing limit on permissible operating voltages [26]. Hot electrons injected into the SiO 2 above high electric fields are illustrated by the diagram below and this explains why the HCI increases carrier damage and why TDDB lifetime decreases exponentially with voltage and increasing field and this limits operating voltages.

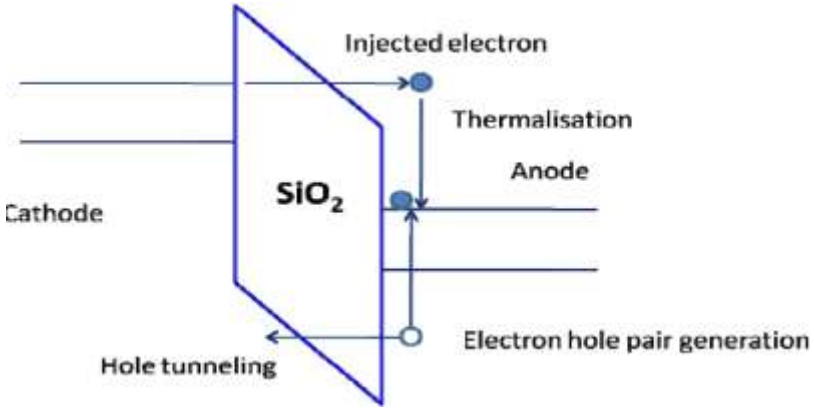


Figure 1. TDDB model [27]

Self-heating also amplifies the processes in 3D architectures by enhancing defects and charge trapping. Trapping related instabilities and degradation of the gate oxide predominate in the case of wide-bandgap devices [28]. In the case of memristive devices, variability in endurance and filament formation during stochastic formation essentially prevents predictability [29]

Application Domains

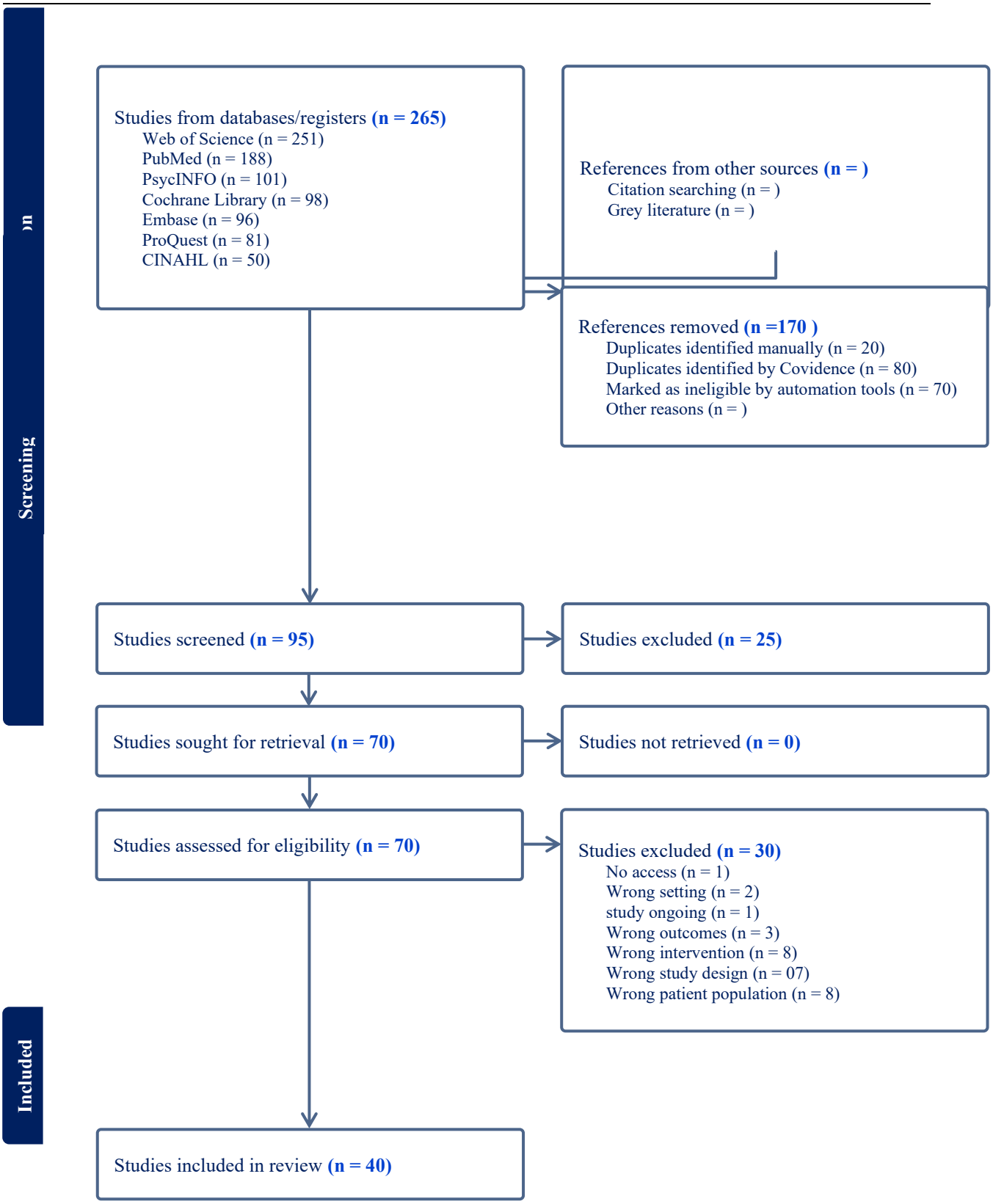
The appropriateness of new semiconductor technology is not only application-oriented, but the technology becomes less general in most cases. The focus of HPC and AI accelerators is on density and energy efficiency, preference on GAAFET logic and high-order 3D integration, but within a rigid set of thermal and reliability constraints. IoT and edge electronics focus on the need of ultra-low power and resistance to variability, where memristive and 2D-based frameworks are potentially useful [30].

GaN and SiC devices are generalized in automotive and power systems as they are more efficient and can operate at higher voltages, although their cost of fabrication and reliability qualification requirements are higher. Flexible electronics are still limited through low-temperature processing and mechanical reliability and cannot directly use high-level logic devices.

Review Methodology

The methodological approaches applied in this review are PRISMA-based, thus all peer-reviewed literature on next-generation semiconductor devices has been systematically identified, screened, and synthesized. It has an adapted approach to the heterogeneity of device architectures, materials, fabrication processes, and reliability metrics that define the modern semiconductor research. Seeing that even no standardized testing conditions exist among the classes of devices, a formal meta-analysis was not themselves used but a structured qualitative synthesis.

The search in literature was accompanied by the utilization of IEEE Xplore, ScienceDirect (Elsevier), SpringerLink, Nature Portfolio journals, ACS Publications [31], the search has been made over the years 2019-2025. This period reflects the recent progress of interest in the areas of advanced logic scaling, wide-bandgap power electronics, and new non-von-Neumann devices. Search queries were a combination of architecture-specific keywords with fabrication and reliability keywords so that performance, process integration and degradation mechanisms would be equally covered.



This review applied PRISMA screening to evaluate nursing-led pediatric health promotion in low-resource communities. From 265 identified records, 95 studies were screened after duplicate removal. Seventy full-text articles were assessed for eligibility, with 30 excluded due to wrong population, setting, or intervention. Ultimately, 40 studies were included, providing evidence on early disease prevention outcomes, caregiver education, and effectiveness of nurse-led community-based

interventions.

Inclusion criteria involved that the studies should report one of the following: quantitative methodologies of device performance, fabrication or integration specifications, or experimentally valid reliability performance. The consideration was limited to peer-review articles and contributions of high impact conference papers. Articles devoted to incremental or legacy planar CMOS technologies not related to next-generation scaling problems were eliminated, and papers that could not be reproduced methodologically were also removed [32].

Selection of the studies was done in two stages. Titles and abstracts were first filtered by eliminating off-scope, and then full-text by checking that the material was relevant and analytical in depth. Analyzed data were performed by comparative synthesis associating performance-reliability tradeoffs and technology preparedness, and not singular performance measurements.

Data Synthesis Framework

Data synthesis was organized in such a way that it would be possible to make a comparison between technologies and to directly answer the research questions and objectives of the study. Scaling benefits, enablers of fabrication that are primarily based on 2D-material FinFET, GAAFET, CFET, 2D-material FET, GaN/SiC power devices, and memristive systems were assessed. This level-level comparison allows finding the basic bottlenecks that will limit further performance improvement.

Table 1. Comparative Analysis of Next-Generation Semiconductor Device Architectures

Device Architecture	Primary Scaling Advantage	Key Fabrication Enablers	Dominant Performance Benefits	Major Reliability / Integration Bottlenecks	Technology Readiness
FinFET	Improved electrostatic control over planar CMOS	Multiple patterning, Fin etch, HKMG	Moderate leakage reduction; mature performance	Fin width variability; parasitic resistance at advanced nodes	Mature (legacy for sub-7 nm)
GAAFET (Nanosheet/Nanowire)	Full gate control; tunable channel width	EUV lithography, ALD gate stacks, selective nanosheet release	Superior leakage suppression; improved SS and short-channel control	Self-heating, stacked-channel variability, tight process windows	Transitional (3–2 nm nodes)
CFET (Monolithic 3D CMOS)	Vertical density scaling beyond planar limits	Sequential device stacking, selective etching, 3D integration	Significant footprint reduction; potential PPA gains	Thermal coupling, alignment complexity, cumulative reliability risk (Leitenberger & Matthiesen, 2024)	Emerging (research / early pilot)
2D-Material FETs	Ultimate body thickness; immunity	Low-defect growth/transfer, contact	Excellent electrostatics; low off-state leakage	High contact resistance; wafer-scale variability;	Experimental

Device Architecture	Primary Scaling Advantage	Key Fabrication Enablers	Dominant Performance Benefits	Major Reliability / Integration Bottlenecks	Technology Readiness
	to short-channel effects	engineering, ALD interfaces		stability issues	
GaN Power Devices	High breakdown field; high switching frequency	Epitaxial growth, passivation, field plates	High efficiency; fast switching for power conversion	Trapping effects; dynamic R_ON degradation	Mature (power & RF)
SiC Power Devices	Wide bandgap; high thermal robustness	High-quality gate oxides, implantation, annealing	High-voltage operation; low conduction losses	Gate oxide reliability; threshold instability	Mature (automotive & energy)
Memristive / RRAM Devices	In-memory computing; analog state storage	Nanoscale filament control, BEOL compatibility	Energy-efficient neuromorphic computation	Endurance limits; stochastic variability	Emerging (AI / edge research)

Techniques like EUV lithography, atomic layer deposition, selective etching and 3D heterogeneous integration were overlaid on technology device architectures as a means to evaluate their enabling capability and risk factors. This/summation is to point out that as the process windows get smaller and stochastic effects gain influence, variability and loss in the advanced equipment become more pronounced.

Reliability was synthesized through technologies in order to detect common physical drivers, such as interface defect generation, high-field stress, thermal acceleration, and stochastic switching [33]. The framework puts reliability above the qualification issue by associating these mechanisms with manifestations of degradation.

Lastly, the suitability of the applications was evaluated through mapping the device classes to major areas, which were high-performance computing, AI accelerators, IoT and edge electronics, automotive power systems, and flexible electronics. This discussion underlines the fact that reliability and thermal control are becoming more crucial factors that govern the application readiness rather than scaling performance on the nominal basis only.

Results (Synthesis)

This section will summarize the evidence reviewed to compare how the new classes of semiconductor devices can be used to transfer architectural and fabrication progress into quantifiable performance and implementation competency. Instead of reporting independent metrics it focuses the results more on cross-technology trends, indicating where performance improvements have been maintained, and where reliability, variability and thermal constraints limit the improvements [34].

Table 2. Synthesis of Performance and Reliability Outcomes across Device Classes

Device Class	Demonstrated Advantage	Evidence from Literature	Dominant Limitation	Overall Outcome
GAAFETs	Improved electrostatics and leakage suppression	Reduced subthreshold swing and improved short-channel control	Self-heating, stacked-channel variability, tight process windows	Clear performance gains with reliability-

Device Class	Demonstrated Advantage	Evidence from Literature	Dominant Limitation	Overall Outcome
		compared to FinFETs [35]		constrained scaling
2D-FETs	Ultimate channel thickness enables strong electrostatic control	Low off-state leakage and steep SS in controlled experiments	High contact resistance, poor wafer-scale reproducibility	High theoretical promise but low near-term scalability
GaN Power Devices	High switching efficiency and breakdown voltage	Demonstrated high power density and efficiency in RF and power electronics	Trapping-induced dynamic degradation	Strong deployment suitability despite reliability trade-offs
SiC Power Devices	High thermal and voltage robustness	Stable operation in high-temperature automotive environments	Gate oxide degradation and threshold drift	Mature technology with ongoing reliability refinement
Memristive Devices	Compute-in-memory capability	Energy-efficient inference and neuromorphic demonstrations	Endurance variability and stochastic switching	Promising for edge AI; limited large-scale reliability

Interpretation

The obtained results show that GAAFET architectures are capable of scaling the electrostatic scaling limit, which validates that GAAFET architectures are the master logic device at advanced nodes. Nevertheless, the advantages are rapidly becoming counterbalanced by self-heating and variability which limits the scaling of voltage and frequency. Conversely, 2D-FETs are currently constrained by their manufacturability, not technical capability and that is why they are still simply demonstrated in experiments.

Table 3. Application Alignment and Technology Readiness

Device Class	Primary Application Domain	Performance Driver	Reliability Constraint	Readiness Level
GAAFETs	HPC and advanced logic	Leakage control and density scaling	BTI, self-heating, variability	Transitional
2D-FETs	Future ultra-scaled logic	Atomic-scale electrostatics	Contact resistance and stability	Experimental
GaN Devices	Power electronics and RF	High efficiency and fast switching	Charge trapping effects	Mature
SiC Devices	Automotive and energy systems	High voltage and thermal stability	Gate oxide reliability	Mature
Memristors	Edge AI and neuromorphic systems	In-memory computing efficiency	Endurance and variability	Emerging

Interpretation.

Application mapping shows that the level of technology preparedness is very domain specific. Wide-bandgap devices have reached commercial maturity due to their material benefits being directly relevant to power and automotive needs, and further improvement of the reliability is compounded in logic-centric innovations.

Table 4. Cross-Cutting Barriers to Next-Generation Device Scaling

Limitation	Affected Technologies	Observed Impact	Scaling Consequence
Variability	GAAFETs, 2D-FETs, Memristors	Parameter dispersion and yield loss	Reduced usable voltage margins
Self-heating	GAAFETs, CFETs	Accelerated aging and thermal throttling	Performance density ceiling
Contact resistance	2D-FETs	Dominates total device resistance	Suppresses performance gains
Endurance degradation	Memristors	State instability and failure	Limits system-level deployment

Interpretation.

Variability and thermal effects are nearly universally found to be the main blockers, even more so than lithographic resolution is the critical scaling limit. This change highlights the importance of architecture and fabrication co-optimization, which is reliability-conscious in development in a future technology.

On the whole, the findings indicate that although building projects have achieved the task of scaling electrostatics, reliability and thermal constraints have become the limiting factors of the next-generation semiconductor technologies. Designs which parallelise material benefits in relation to application specific needs (GaN or SiC) are more ready [36], but advances in logic design are confronted with more and more non-idealities to manage through progressive acquisitions of fabrication control and predictive reliability models.

4. Discussion

The findings provide a picture that further dependence on EUV lithography is approaching a practicality that is beyond the resolution of patterns. Despite the fact that EUV has made it possible to pattern at advanced nodes in a single pattern, stochastic effects, resist variability and cost continue to rise, limiting yield and manufacturability ever-increasingly [37]. With the scaling of architecture and geometry of the devices into three-dimensions, none of the marginal lithographic advances deliver linear gains to performance, changing the scaling problem into robustness to process variations and defect tolerance.

Meanwhile, the method of atomic layer deposition (ALD) that is required in the conformal gate stack and spacer of GAAFET and 3D device construction is being constrained with closed process windows. Scatter in precursor chemistry, interface quality and uniformity in thickness have an increasingly large effect on device variability and long term reliability. These are disadvantageous to aggressive scaling of the same oxide thickness and difficult to integrate heterogeneous materials, especially in vertically stacked applied.

The shift to 3D device designs such as stacked nanosheet GAAFET designs and CFET designs have increased the contribution of self-heating to the primary performance limitation of first-order. Vertical integration in channels thermally coupled also increases the rate of degradation processes like BTI, TDDB and limits the scaling of voltages and frequencies. The results indicate that the capability to address thermal management and not electrostatics is gradually becoming the defining characteristic of performance envelope of next-generation logic devices.

In all of the considered technologies, reliability becomes the most important bottleneck below

the 3 nm regime [38]. Even though architectural developments are still providing nominal performance increases, reduced reliability negatively affects the available operating ranges and eliminates lifetime guarantees. The underlying trend leads to a paradigm shift in technology roadmaps as reliability mindful design and qualification becomes more and more the determinant of the need and timing of uptake, along with which application is appropriate.

In this regard, AI-based modeling and forecasting dependable models are likely to be vital. Machine learning solutions can help to speed up optimization cycles and predict the failure mechanisms as well as minimize the expensive experimental reiterations by combining process data, device physics [39], and degradation behavior. These techniques are especially applicable to the 3D integration and material heterogeneous system complexity.

5. Conclusion

Based on this review, it can be seen that next-generation semiconductor devices have made significant advances in scale extending the limits of conventional CMOS scaling in regards to performance and functionality. GAAFET structures, wide-bandgap power devices, and forthcoming technologies of neuromorphic, each have different applications requirements, which proves that the future of scaling will not be universal and will be application-driven. Nevertheless, the results are uniformly consistent where scalability and reliability issues are close-knit to the full usage of architectural and fabrication developments.

The focus of future investigations should thus be on monolithic 3D integration (vertical stacking) that contributes to the density advantage without correspondingly raising the footprint in proportion with such enhancement, and mitigates the thermal and reliability issues. Simultaneously, carbon-based electronics, such as 2D materials, and carbon nanotubes remain long-term potential in terms of minuscule channels, intra-connections, the alternative can be solved through the manufacturability, stability of contact, etc. In addition to classical notions of devices, quantum-inspired and non-von-Neumann architectures including memristive and hybrid systems will be useful but will not supplant CMOS since they address energy-efficient computation.

Lastly, AI aided device and process design will be one of the core agents of next-generation semiconductor innovation. Through predictive reliability and modeling of performance and incorporating them into early phases of design, AI-centered solutions can reduce the development process and enhance the technological preparedness. Comprehensively, long-term advances in semiconductor technology will require fewer advances based on incremental scaling and rely more upon integrated optimization of architecture, fabrication and reliability.

References

[1] H. H. Radamson *et al.*, "CMOS scaling for the 5 nm node and beyond: Device, process and Technology," *Nanomaterials*, vol. 14, no. 10, p. 837, 2024, doi: 10.3390/nano14100837.

[2] H. Duan, "From MOSFET to FinFET to GAAFET: The evolution, challenges, and future prospects," *Applied and Computational Engineering*, vol. 50, no. 1, pp. 113–120, 2024, doi: 10.54254/2755-2721/50/20241285.

[3] J. Sangid, G. Long, P. Mitchell, B. J. Blalock, D. J. Costinett, and L. M. Tolbert, "Comparison of 60v gan and SI devices for Class D Audio Applications," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 73–76. doi: 10.1109/wipda.2018.8569105.

[4] L. Zhang *et al.*, "Global trends in intestinal flora and ulcerative colitis research during the past 10 years: A bibliometric analysis," *Front. Med. (Lausanne).*, vol. 13, p. 1003905, 2022.

[5] J. W. McPherson, "Four decades of E-model development for time-dependent dielectric breakdown (TDDB)," *IEEE Electron Devices Reviews*, pp. 1–10, 2025, doi: 10.1109/edr.2025.3620381.

[6] O. Prakash, C. K. Dabhi, Y. S. Chauhan, and H. Amrouch, "Transistor self-heating: The rising challenge for semiconductor testing," in *2021 IEEE 39th VLSI Test Symposium (VTS)*, 2021. doi: 10.1109/vts50974.2021.9441002.

[7] Capital Markets Authority, "Annual Report and Financial Reports," 2016.

[8] L. Wong, G. W. Tan, K. Ooi, B. Lin, and Y. K. Dwivedi, "Artificial intelligence-driven risk management for enhancing supply chain agility: A deep-learning-based dual-stage PLS-SEM-ANN analysis," *Int. J. Prod. Res.*, vol. 62, no. 15, pp. 5535–5555, 2022, doi: 10.1080/00207543.2022.2063089.

[9] Nanosheet, "Nanoscale Memristor Device and Circuits Design," 2024, doi: 10.1016/c2020-0-04178-2.

[10] M. Balasubbareddy, K. Sivasankaran, A. E. Atamuratov, and M. M. Khalilloev, "Optimization of vertically stacked nanosheet fet immune to self-heating," *Micro and Nanostructures*, vol. 182, p. 207633, 2023, doi: 10.1016/j.micrna.2023.207633.

[11] Nano, "Gaafet vs finfet: 'transistoring' to all-around nanosheets," 2025. [Online]. Available: https://techlevated.com/gaafet-vs-finfet-transistor/

[12] C. Dutta, A. Dastidar, and K. C. Bhuyan, "Low power design technology from mosfets to cfets," in *Exploring the Intricacies of Digital and Analog VLSI*, 2025, pp. 1–48. doi: 10.4018/979-8-3693-8084-0.ch001.

[13] A. Bhardwaj *et al.*, "Comprehensive analysis on complementary fet," *IEEE Access*, vol. 13, pp. 82554–82572, 2025, doi: 10.1109/access.2025.3568134.

[14] C.-S. Pang, P. Wu, J. Appenzeller, and Z. Chen, "Thickness-dependent study of high- performance WS2-fets with ultrascaled channel lengths," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2123–2129, 2021, doi: 10.1109/ted.2021.3058078.

[15] A. P. Jacob, R. Xie, M. G. Sung, L. Liebmann, R. T. Lee, and B. Taylor, "Scaling challenges for advanced CMOS devices," *International Journal of High Speed Electronics and Systems*, vol. 26, no. 01n02, p. 1740001, 2017, doi: 10.1142/s0129156417400018.

[16] F. Roccaforte *et al.*, "Recent advances on dielectrics technology for SIC and Gan Power Devices," *Appl. Surf. Sci.*, vol. 301, pp. 9–18, 2014, doi: 10.1016/j.apsusc.2014.01.063.

[17] M.-K. Song *et al.*, "Recent advances and future prospects for memristive materials, devices, and systems," *ACS Nano*, vol. 17, no. 13, pp. 11994–12039, 2023, doi: 10.1021/acsnano.3c03505.

[18] D. Kazazis, J. G. Santaclara, J. van Schoot, I. Mochi, and Y. Ekinci, "Extreme ultraviolet lithography," *Nature Reviews Methods Primers*, vol. 4, no. 1, 2024, doi: 10.1038/s43586-024-00361-z.

[19] D. Zhao *et al.*, "T helper cell 17/regulatory T cell balance regulates ulcerative colitis and the therapeutic role of natural plant components: a review," *Front. Med. (Lausanne).*, vol. 11, p. 1502849, 2024, doi: 10.3389/fmed.2024.1502849.

[20] S. Zhang, R. Zhong, S. Tang, L. Chen, and H. Zhang, "Metabolic regulation of the Th17/Treg balance in inflammatory bowel disease," *Pharmacol. Res.*, vol. 203, p. 107184, 2024.

[21] X. Chevalier, B. Parvais, and J.-P. Raskin, "Selective etching challenges for nanosheet devices," *Microelectron. Eng.*, vol. 195, pp. 24–30, 2018, doi: 10.1016/j.mee.2018.03.003.

[22] J.-Q. Lu, R. J. Gutmann, and D. McHerron, "Monolithic 3D integration: Opportunities and challenges," *IEEE Des. Test*, vol. 38, no. 2, pp. 54–63, 2021, doi: 10.1109/MDAT.2020.3026871.

[23] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of GAAFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5494–5501, 2020, doi: 10.1109/TED.2020.3031765.

[24] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014, doi: 10.1109/TPEL.2013.2268900.

[25] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Res.*, vol. 3, no. 3, pp. 147–169, 2010, doi: 10.1007/s12274-010-1019-z.

[26] C. Hu, Y.-H. Lin, and M. Lee, "Reliability challenges in advanced CMOS technologies," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3527–3535, 2018, doi: 10.1109/TED.2018.2850778.

[27] D. Ielmini and H.-S. P. Wong, "In-memory computing with resistive switching devices," *Nat. Electron.*, vol. 1, no. 6, pp. 333–343, 2018, doi: 10.1038/s41928-018-0092-2.

[28] A. K. Agarwal, S. Haney, S.-H. Ryu, and J. W. Palmour, "Reliability issues in SiC power devices," *IEEE Transactions on Device and Materials Reliability*, vol. 20, no. 2, pp. 216–227, 2020, doi: 10.1109/TDMR.2020.2980201.

[29] D. Ielmini and H.-S. P. Wong, "In-memory computing with resistive switching devices," *Nat. Electron.*, vol. 1, no. 6, pp. 333–343, 2018, doi: 10.1038/s41928-018-0092-2.

[30] D. Markovic, A. Mizrahi, D. Querlioz, and J. Grollier, "Physics for neuromorphic computing," *Nature Reviews Physics*, vol. 2, no. 9, pp. 499–510, 2020, doi: 10.1038/s42254-020-0208-2.

[31] B. N. Chigarev, "On Visual Data Analysis of IEEE Xplore Bibliometric Records on machine learning and Artificial Intelligence for Power Systems," *Energy Systems Research*, vol. 8, no. 1(29), pp. 12–29, 2025, doi: 10.25729/esr.2025.01.0002.

[32] D. Castelvecchi, "Preprint site arxiv is banning computer-science reviews: Here's why," *Nature*, 2025, doi: 10.1038/d41586-025-03664-7.

[33] Reliability, R. Physics, and P., *Applied Engineering on physics-of-healthy and SHM of microelectronic equipment for aeronautic, space, automotive and Transport Operations*. 2022. doi: 10.1002/9781394186068.ch2.

[34] S. Sarkar, "CFD-based investigation of heat transfer efficiency in renewable energy systems," *International Journal of Scientific Interdisciplinary Research*, vol. 01, no. 01, pp. 129–162, 2022, doi: 10.63125/ttw40456.

[35] K. Patel, N. Vala, M. Limachia, and P. Dalal, "Comprehensive study of short channel effects (sces) in MOSFET and FinFET devices," in *Communications in Computer and Information Science*, 2024, pp. 133–144. doi: 10.1007/978-3-031-75170-7_10.

[36] T. P. Chow, "S4-P1: Wide and extreme bandgap semiconductor devices for power electronics applications," in *2014 Lester Eastman Conference on High Performance Devices (LEC)*, 2014, pp. 1–4. doi: 10.1109/lec.2014.6951567.

[37] T. Bauer, A. Jones, A. Lentine, J. Mudrick, M. Okandan, and A. Rodrigues, "Trends in Microfabrication Capabilities & Device Architectures," 2015. doi: 10.2172/1192538.

[38] Q. Teng, Y. Hu, R. Cheng, Y. Wu, G. Zhou, and D. Gao, "Reliability challenges in CMOS technology: A manufacturing process perspective," *Microelectron. Eng.*, vol. 281, p. 112086, 2023, doi: 10.1016/j.mee.2023.112086.

[39] Y. Li, G. Lei, G. Bramerdorfer, S. Peng, X. Sun, and J. Zhu, "Machine learning for design optimization of electromagnetic devices: Recent developments and Future Directions," *Applied Sciences*, vol. 11, no. 4, p. 1627, 2021, doi: 10.3390/app11041627.